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## PERP. TO FIN VIEW

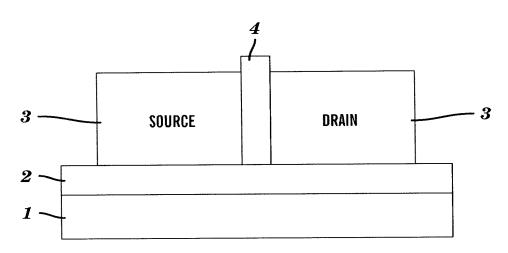


FIG. 1 PRIOR ART

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## PARALLEL TO FIN VIEW

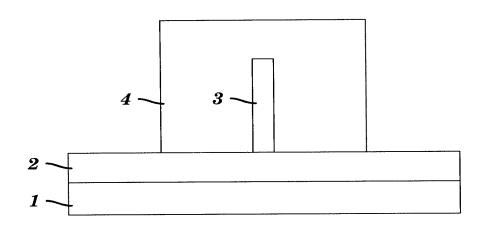
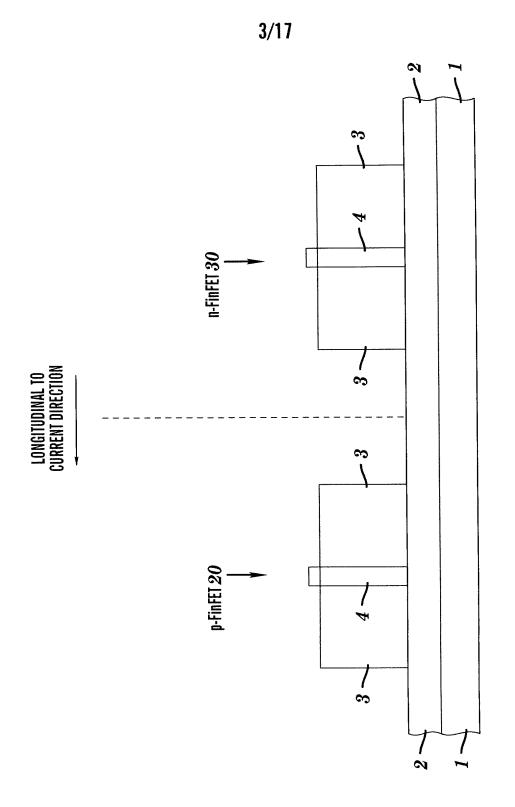


FIG. 2 PRIOR ART





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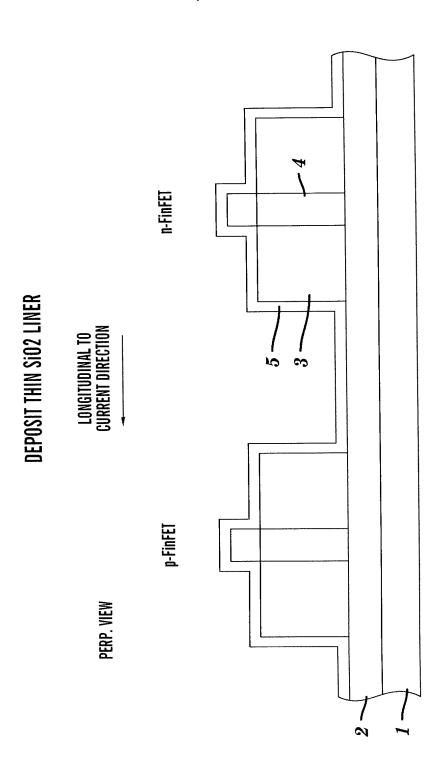


FIG. 4

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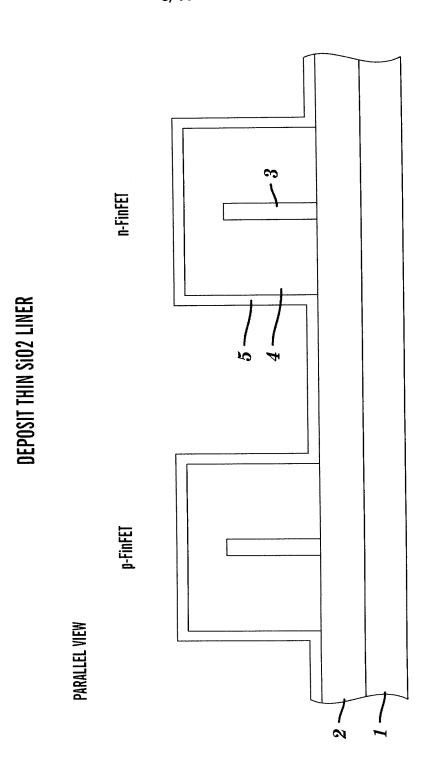
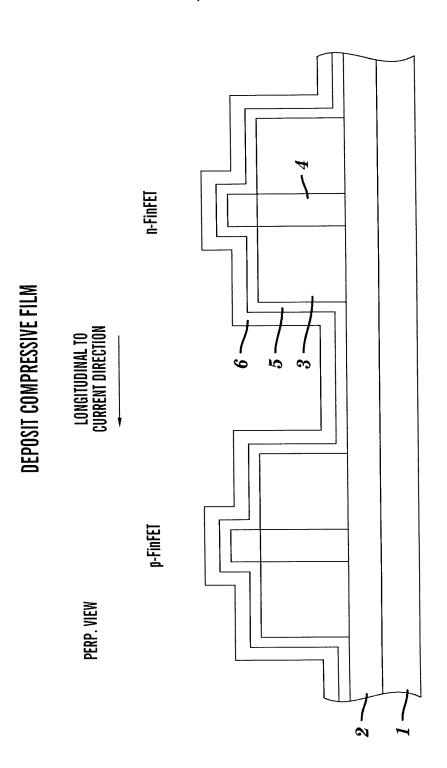


FIG. 5

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 $FIG. \ 6$ 

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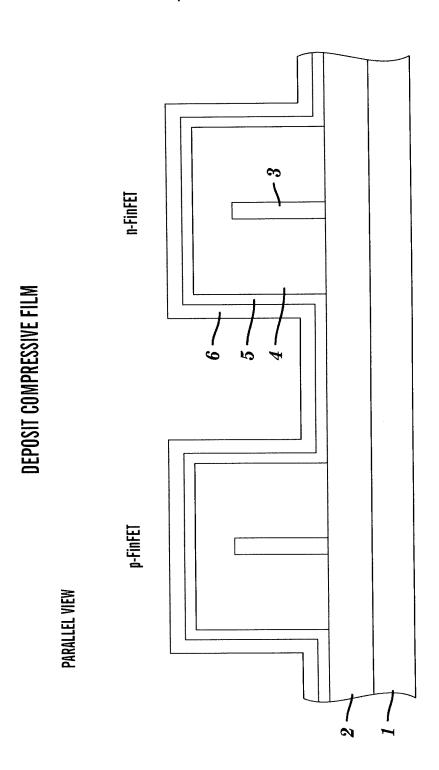


FIG. 7

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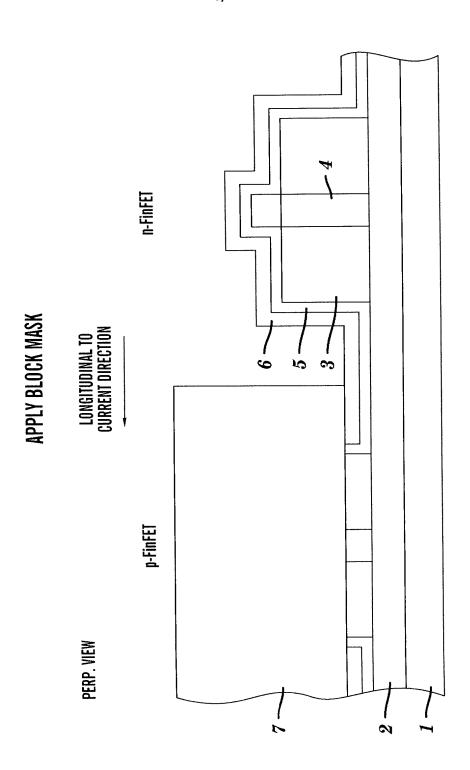


FIG. 8

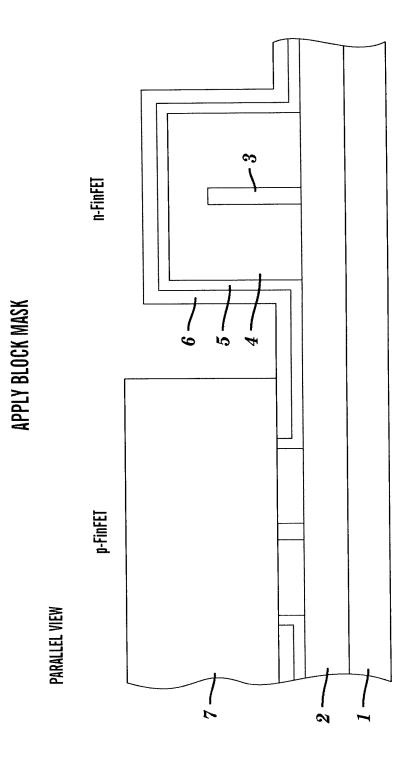


FIG. 9

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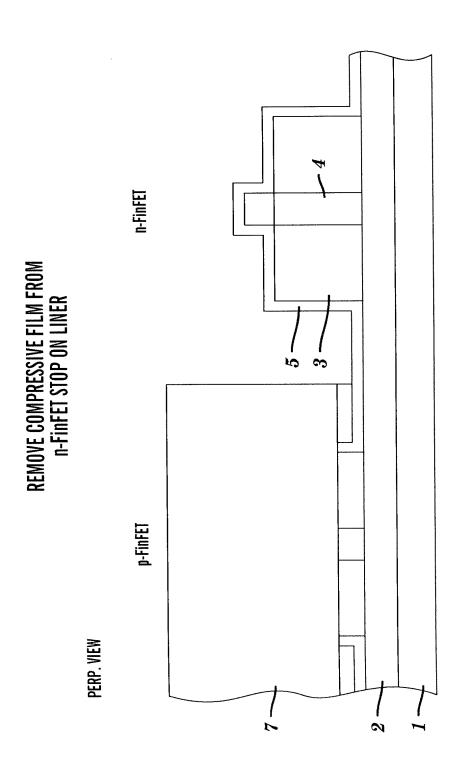


FIG. 10

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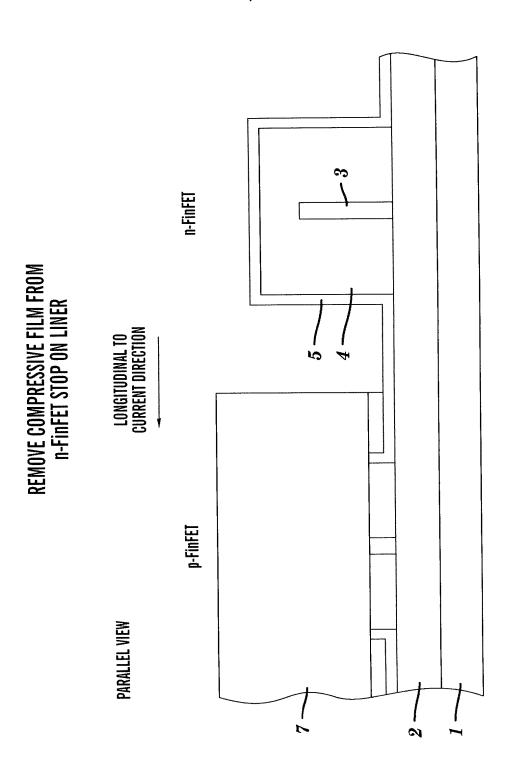


FIG. 11

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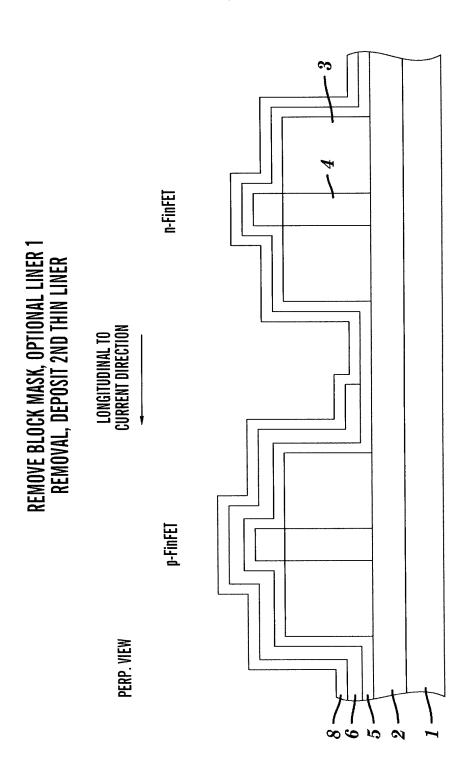


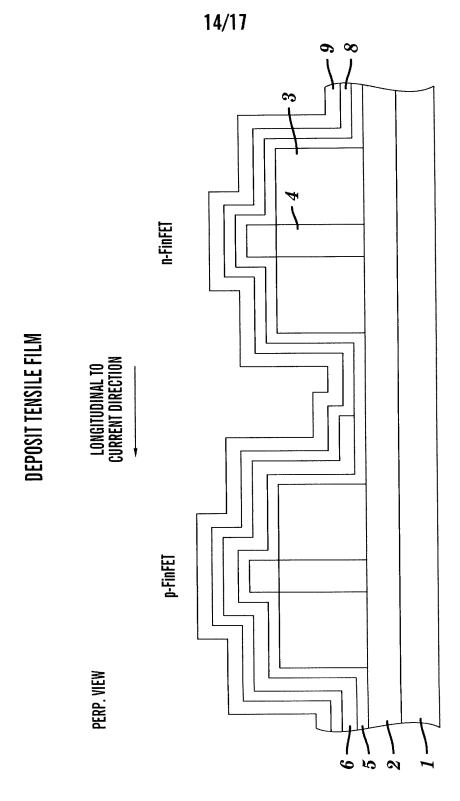
FIG. 12

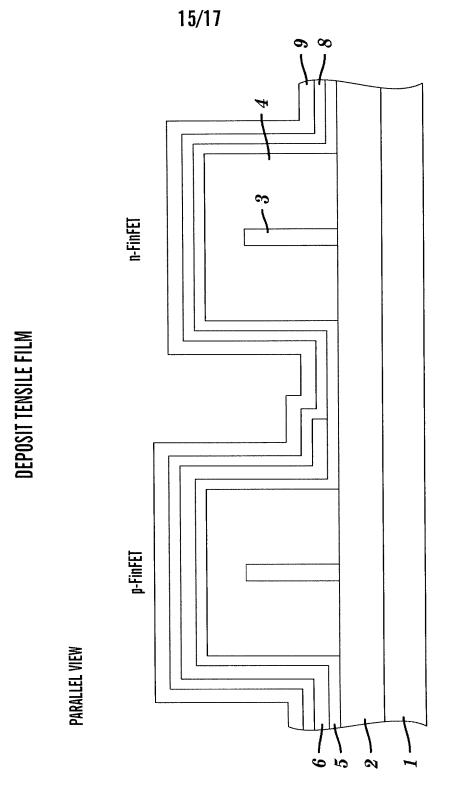
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n-FinFET REMOVE BLOCK MASK, OPTIONAL LINER 1 REMOVAL, DEPOSIT 2ND THIN LINER p-FinFET PARALLEL VIEW 0000

FIG. 13

FIG. 14





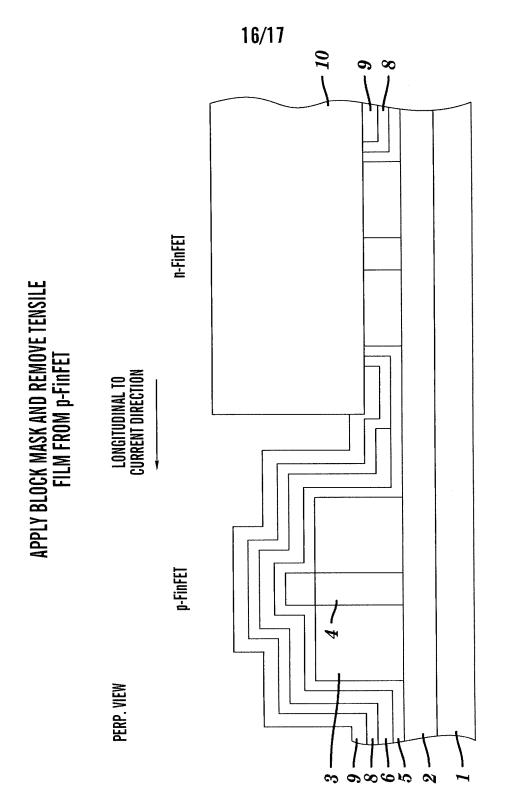


FIG. 16

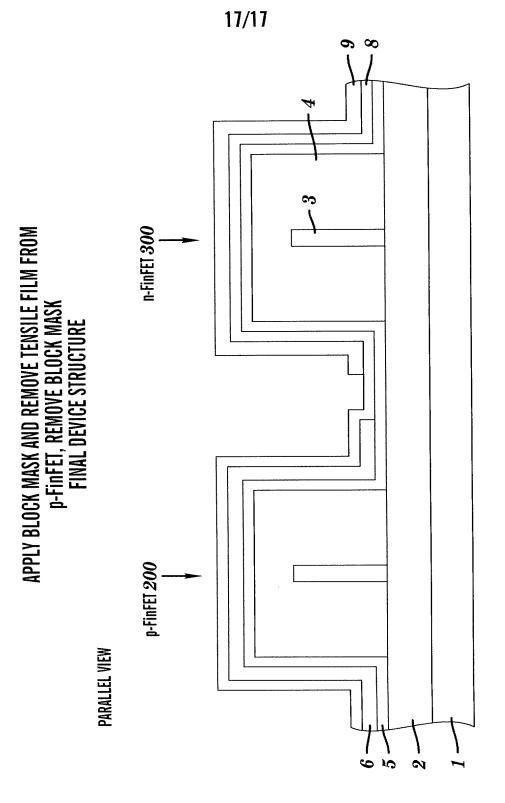


FIG. 17